1 Instruction set extensions for software defined radio on a multithreac

Suman Mamidi, Emily R. Blem, Michael J. Schulte, John Glossner, Daniel Ia Iancu, Mayan Moudgill, Sanjay Jinturkar

September 2005 **CASES '05:** Proceedings of the 2005 international conferer Compilers, architectures and synthesis for embedded syste

Publisher: ACM

Full text available: Pdf (189.05 KB) Additional Information: full citation, abstract, referen

Bibliometrics: Downloads (6 Weeks): 8, Downloads (12 Months): 57, Citation (

Software defined radios, which provide a programmable solution for imp physical layer processing of multiple communication standards, are wid one of the most important new technologies for wireless communication

Keywords: Reed-Solomon coding, Viterbi decoding, convolutional enco signal processor, forward error correction, instruction set extensions, m software defined radio, turbo decoding

2 Low-power asynchronous viterbi decoder for wireless applications

Mohamed Kawokgy, C. André T. Salama

August 2004 **ISLPED '04:** Proceedings of the 2004 international symposiun electronics and design

Publisher: ACM

Full text available: Pdf (220.30 KB) Additional Information: full citation, abstract, referen terms

Bibliometrics: Downloads (6 Weeks): 1, Downloads (12 Months): 21, Citation (

This paper describes the implementation of an asynchronous 64-state, decoder using an original architecture and design methodology. The dec for wireless communications applications, where bit rates over 100 Mb/s minimum ...

Keywords: VHDL, asynchronous, bundled-data, digital signal processin handshaking protocol, low-power, register transfer level, speed-indepen synchronous, viterbi algorithm, wireless

3 Low power architecture of the soft-output Viterbi algorithm

David Garrett, Mircea Stan

August 1998 **ISLPED '98:** Proceedings of the 1998 international symposiun electronics and design

Publisher: ACM

Full text available: Pdf (758.59 KB) Additional Information: full citation, abstract, referen terms

Bibliometrics: Downloads (6 Weeks): 2, Downloads (12 Months): 36, Citation (

An important technique for reducing pow er consumption in VLSI systen reduction, the substitution of a less-costly operation such as a shift, for operation such a multiplication. Using a logarithmic number represen ta

Keywords: SOVA, VA, low power, turbo codes

4 Reconfigurable platforms for ubiquitous computing

Manfred Glesner, Thomas Hollstein, Leandro Soares Indrusiak, Peter Zipf, Mihail Petrov, Heiko Zimmer, Tudor Murgan

April 2004 **CF '04:** Proceedings of the 1st conference on Computing frontier

Publisher: ACM

Full text available: Pdf (479.97 KB) Additional Information: full citation, abstract, referen

Bibliometrics: Downloads (6 Weeks): 6, Downloads (12 Months): 100, Citation

Ubiquitous computing requires flexibilty. Melting distributed electronic d everyday's life implies the need to adapt to evolving standards and dyn environments. Furthermore, to gain user acceptance, such devices shou adapt ...

Keywords: communication, dynamic power management, networks-on reconfigurable hardware, reconfigurable processors, reconfiguration, ub computing

5 A low power Viterbi decoder implementation using scarce state trans pruning scheme for high throughput wireless applications

Jie Jin, Chi-Ying Tsui

October 2006 **ISLPED '06:** Proceedings of the 2006 international symposiu electronics and design

Publisher: ACM

Full text available: Pdf (332.13 KB) Additional Information: full citation, abstract, referen

Bibliometrics: Downloads (6 Weeks): 7, Downloads (12 Months): 69, Citation (

This paper presents a low power Viterbi decoder design based on Scarc Transition (SST). We propose an approach which seamlessly integrates techniques with the SST decoding to reduce the average add-compare-s computation. ...

Keywords: Viterbi algorithm, convolutional code, low power

6 MetaCores: design and optimization techniques

Seapahn Meguerdichian, Farinaz Koushanfar, Advait Morge, Dusan Petrano Potkonjak

June 2001 **DAC '01:** Proceedings of the 38th conference on Design automa

Publisher: ACM

Full text available: Pdf (283.78 KB) Additional Information: full citation, abstract, referen terms

Bibliometrics: Downloads (6 Weeks): 10, Downloads (12 Months): 42, Citation

Currently, hardware intellectual property (IP) is delivered at three level: hard, firm, and soft. In order to further enhance performance, efficiency of IP design, we have developed a new approach for designing hardwar

7 Design of low-power high-speed maximum a priori decoder architect
A. Worm, H. Lamm, N. Wehn
March 2001 **DATE '01:** Proceedings of the conference on Design, automatic Europe
Publisher: IEEE Press
Full text available: Pdf (129.21 KB) Additional Information: full citation, references, cited

Bibliometrics: Downloads (6 Weeks): 1, Downloads (12 Months): 9, Citation C

8 Vectorizing for a SIMdD DSP architecture
Dorit Naishlos, Marina Biberstein, Shay Ben-David, Ayal Zaks
October 2003 **CASES '03:** Proceedings of the 2003 international conference architecture and synthesis for embedded systems
Publisher: ACM
Full text available: Pdf (301.45 KB) Additional Information: full citation, abstract, referen terms

Bibliometrics: Downloads (6 Weeks): 3, Downloads (12 Months): 60, Citation (

The Single Instruction Multiple Data (SIMD) model for finegrained parall recently extended to support SIMD operations on disjoint vector elemen we demonstrate how SIMdD (SIMD on disjoint data) supports e# ective

Keywords: SIMD, compiler controlled cache, data reuse, rotating regis parallelism, vectorization, viterbi

9 VLSI implementation of SISO arithmetic decoders for joint source ch
Simone Zezza, Guido Masera
March 2008 **DATE '08:** Proceedings of the conference on Design, automatic Europe
Publisher: ACM
Full text available: Pdf (129.33 KB) Additional Information: full citation, abstract, referen

Bibliometrics: Downloads (6 Weeks): 4, Downloads (12 Months): 10, Citation (

In this paper we propose an efficient VLSI implementation of a Soft Inp (SISO) arithmetic code (AC) decoder for joint source channel coding. Th application shows a very high level of processing complexity, but, to the

10 A dynamically reconfigurable adaptive viterbi decoder
Sriram Swaminathan, Russell Tessier, Dennis Goeckel, Wayne Burleson
February 2002 **FPGA '02:** Proceedings of the 2002 ACM/SIGDA tenth intern symposium on Field-programmable gate arrays
Publisher: ACM
Full text available: Pdf (235.26 KB) Additional Information: full citation, abstract, referen

Bibliometrics: Downloads (6 Weeks): 8, Downloads (12 Months): 70, Citation (

The use of error-correcting codes has proven to be an effective way to c corruption in digital communication channels. Although widely-used, the communications decoding algorithm, the Viterbi algorithm, requires an

Keywords: FPGA, Viterbi coding, dynamic reconfiguration

11 A reconfigurable application specific instruction set processor for cor turbo decoding in a SDR environment

Timo Vogt, Norbert Wehn

March 2008 **DATE '08:** Proceedings of the conference on Design, automatic Europe

Publisher: ACM

Full text available: Pdf (527.34 KB) Additional Information: full citation, abstract, referen

Bibliometrics: Downloads (6 Weeks): 11, Downloads (12 Months): 60, Citation

Future mobile and wireless communication networks require flexible mo architectures to support seamless services between different network st a common hardware platform that can support multiple protocols imple controlled by ...

12 BER evaluation and rate matching attribute selection for QoS suppor downlink

Joy Kuri, R. M. Karthik

December 2008 **Wireless Networks** , Volume 14 Issue 6

Publisher: Kluwer Academic Publishers

Full text available: Pdf (429.61 KB) Additional Information: full citation, abstract, referen

Bibliometrics: Downloads (6 Weeks): 4, Downloads (12 Months): 35, Citation (

In UMTS technology, Coded Composite Transport Channels (CCTrCh-s) multiple Transport Channels (TrCh-s) in parallel on (usually) one physic connection. Rate Matching Attributes (RMA-s) are used to share the CC among ...

Keywords: UMTS, bit/frame error rate, mobile communication systems systems, rate matching attributes, wireless communication